In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method of operating an integrated circuit including read accessible memory comprising the steps of:

testing memory read operations beginning at a maximum speed at successively slower speeds until all memory reads pass;

determining memory read program bits for a highest memory speed passing the memory read tests; and

programming write once bits according to determined memory read program bits.

2. (Original) The method of claim 1 further comprising the steps of:

preliminary soft programming determined bits; and

testing non-memory portions of the integrated circuit using soft programmed determined memory read program bits.

3. (Original) The method of claim 1 wherein:

said step of programming write once bits includes

applying program voltages to the bits,

testing the write once bits to determine achieved programming, and

repeating applying program voltages and testing the write once bits until the testing confirms correct write once bit programming.

4. (Currently Amended) The method of claim 1 wherein programming of ~~eFuse~~ write once bits includes:

merging of programming of write once bits for memory read speed with programming write once bits not related to memory speed.

5. (Original) The method of claim 4 wherein:

the write once bits not related to memory speed include a specific die-identification bit code.

6. (Original) The method of claim 4 wherein:

the write once bits not related to memory read speed include write once bits for memory redundancy programming.

7. (Original) The method of claim 4 wherein:

the write once bits not related to memory read speed include write once bits for control of programmable logic functions.

8. (Original) The method of claim 1, wherein the read accessible memory is write accessible, further comprising:

testing memory write operations beginning at a maximum speed at successively slower speeds until all memory reads pass;

determining memory write program bits for a highest memory speed passing the memory write tests; and

said step of programming write once bits according to determined memory read program bits further includes programming write once bits according determined memory write program bits.

9. (Original) A method of operating an integrated circuit including write accessible memory comprising the steps of:

testing memory write operations beginning at a maximum speed at successively slower speeds until all memory writes pass;

determining memory write program bits for a highest memory speed passing the memory write tests; and

programming write once bits according to determined memory write program bits.

10. (Original) The method of claim 9 further comprising the steps of:

preliminary soft programming determined write once bits; and

testing non-memory portions of the integrated circuit using soft programmed determined memory write program bits.

11. (Original) The method of claim 9 wherein:

said step of programming write once bits includes

applying program voltages to the write once bits,

testing the write once bits to determine achieved programming, and

repeating applying program voltages and testing the write once bits until the testing confirms correct write once bit programming.

12. (Original) The method of claim 9 wherein:

programming of write once bits includes merging of programming of write once bits for memory write speed with programming write once bits not related to memory speed.

13. (Original) The method of claim 12 wherein:

the write once bits not related to memory write speed include a specific die-identification bit code.

14. (Original) The method of claim 12 wherein:

the write once bits not related to memory write speed include write once bits for memory redundancy programming.

15. (Original) The method of claim 12 wherein:

the write once bits not related to memory write speed include write once bits for control of programmable logic functions.

16 to 18. (Canceled)

19. (New) The method of claim 1 further comprising the steps of:

operating memory read operations of the read accessible memory at a speed corresponding to the programmed write once memory read program bits.

20. (New) The method of claim 8 further comprising the steps of:

operating memory write operations of the read accessible memory at a speed corresponding to the programmed write once memory write program bits.

21. (New) The method of claim 9 further comprising the steps of:

operating memory write operations of the write accessible memory at a speed corresponding to the programmed write once memory write program bits.